



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/615,087	07/09/2003	Jong-Bum Park	P68986US0	2392

7590 12/14/2004
JACOBSON, PRICE, HOLMAN & STERN
PROFESSIONAL LIMITED LIABILITY COMPANY
400 Seventh Street, N.W.
Washington, DC 20004

EXAMINER	
WILCZEWSKI, MARY A	
ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 12/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/615,087	PARK, JONG-BUM
	Examiner Mary Wilczewski	Art Unit 2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE THREE MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on ____.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-18 is/are pending in the application.
 - 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) Claim(s) 11-15 and 17 is/are allowed.
- 6) Claim(s) 1, 10, 16, and 18 is/are rejected.
- 7) Claim(s) 2-9 is/are objected to.
- 8) Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on July 9, 2003 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. ____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____ . |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date ____ . | 6) <input type="checkbox"/> Other: ____ . |

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

The drawings filed on July 9, 2003, are acceptable.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Heida, US 6,696,721, or Kwok et al., US 6,429,087, in view of Crenshaw et al., US 2002/0057548.

Kwok et al. disclose a method for fabricating a capacitor in which an interlayer insulation layer 56 is deposited on a substrate 52, a hole 58 is formed in the insulation layer exposing a partial portion of the substrate, a storage node plug 60 is formed in the

hole (see figure 3), a storage node insulation layer 62 having a concave pattern of which the bottom region has a wider critical dimension than that of a top region and which exposes the storage node plug (see figure 5), a lower electrode 80 is formed inside of the concave pattern and connected to the storage node 60 (see figure 6), and a dielectric layer 90 and an upper electrode 92 are sequentially formed on the lower electrode (see figure 10).

Heida disclose a method for fabricating a capacitor in which an interlayer insulation layer 6, 8 is deposited on a substrate 1, a hole is formed in the insulation layer exposing a partial portion of the substrate, a storage node plug 7, 10, 11 is formed in the hole (see figure 4B), a storage node insulation layer 13 having a concave pattern of which the bottom region has a wider critical dimension than that of a top region and which exposes the storage node plug (see figure 15B), a lower electrode 144 is formed inside of the concave pattern and connected to the storage node 7, 10, 11 (see figure 15B), and a dielectric layer 15 and an upper electrode 16 are sequentially formed on the lower electrode (see figure 14B).

Whereas Heida and Kwok et al. teach to form the storage node in a contact hole formed in an interlayer insulation layer, neither Heida or Kwok et al. teach or suggest depositing a stack layer of the interlayer insulation and a first barrier layer. However, Crenshaw et al. discloses that an etch-stop layer 16, i.e., a barrier layer, can be used in etching the contact hole. The etch-stop layer 16 provides a barrier to the etching of the interlayer dielectric layer 14, see paragraphs [0016], [0017], [0019], and [0020]. In light of the teaching of Crenshaw et al., it would have been obvious to one skilled in the art

that an etch-stop layer could have been used in the known method of Heida or Kwok et al. in order to provide a barrier to the etching of the interlayer insulation layer, thereby providing more control over the etching of the contact hole in which the storage node is to be formed.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Heida, US 6,696,721, or Kwok et al., US 6,429,087, in view of Crenshaw et al., US 2002/0057548 as applied to claim 1 above, and further in view of Narwankar et al., US 2002/0168847.

Heida, Kwok et al., and Crenshaw et al. are applied as above. Heida and Kwok et al. lack anticipation of nitridating a surface of the lower electrode. Narwankar et al. disclose nitridating the surface of a metallic layer used to provide the lower electrode of a capacitor in order to provide a stable interface between the metallic layer and a subsequently-formed dielectric layer, see the abstract. Nitridating the surface of the lower electrode of the capacitors formed in the known methods of Heida or Kwok et al. would have been obvious to one skilled in the art in order to provide a stable interface between the lower electrode and the dielectric layer of the capacitor.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 16 and 18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 16 and 18 are duplicates of claims 7 and 9, respectively. Although claim 16 presently depends from claim 2, it appears that this was an inadvertent error and, presumably, Applicant intended claim 16 to depend from claim 12, not claim 2. It is suggested that claim 16 be amended to depend from claim 12.

Allowable Subject Matter

Claims 11-15 and 17 are allowable over the prior art of record.

Claims 2-9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 16 and 18 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

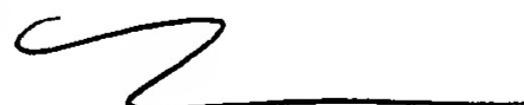
Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The additionally cited references disclose various methods of fabricating a capacitor, some include the step of nitridating the surface of the lower electrode prior to formation of the inter-electrode dielectric layer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary Wilczewski whose telephone number is (571) 272-1849. The examiner can normally be reached on Monday and Thursday.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


M. Wilczewski
Primary Examiner
Tech Center 2800